

**Tribhuvan University**  
**Institute of Science and Technology**  
**Bachelor Level/Second Year/Third Semester/Science**  
**Computer Science and Information Technology (BSc. CSIT)**  
**Course Title: Computer Architecture**  
**Micro-syllabus**

**Course No.:** CSC 201

**Credit hours:** 3hrs.

**Full Marks:** 80+20

**Nature of Course:** Theory (3 hrs.)

**Pass Marks:** 32+8

**Course Synopsis:** This course gives the fundamental knowledge concern with the way the hardware components are connected together to form a computer system and how they interact to provide the processing needs of the user.

**Goals:**

- Introduces the fundamental concepts behind the design working and organization of a computer system.
- Instruction set architecture, memory hierarchies and interconnection.

Unit	Topic	Hrs.
1.	Data representation	5
	<ul style="list-style-type: none"> <li>• Data representation <ul style="list-style-type: none"> <li>➤ Data types – number systems, alphanumeric representation, complements (<math>r</math>'s and <math>r-1</math>'s)</li> </ul> </li> </ul>	1.5
	<ul style="list-style-type: none"> <li>• Fixed point representation <ul style="list-style-type: none"> <li>➤ Integer representation</li> <li>➤ Arithmetic addition, subtraction, overflows.</li> <li>➤ Decimal fixed point representation</li> </ul> </li> </ul>	1
	<ul style="list-style-type: none"> <li>• Floating point representation</li> </ul>	1
	<ul style="list-style-type: none"> <li>• Binary and decimal codes <ul style="list-style-type: none"> <li>➤ Gray, BCD, ASCII, Excess-3</li> </ul> </li> </ul>	1
	<ul style="list-style-type: none"> <li>• Error detection code <ul style="list-style-type: none"> <li>➤ Parity bit, parity checker and parity generator</li> </ul> </li> </ul>	0.5
2.	Micro-operations	5
	<ul style="list-style-type: none"> <li>• Arithmetic micro-operations <ul style="list-style-type: none"> <li>➤ Add micro-operation, subtract micro-operation</li> <li>➤ Binary adder, binary subtractor, binary adder-subtractor, binary incrementor.</li> <li>➤ Arithmetic circuit</li> </ul> </li> <li>• Logic micro-operations <ul style="list-style-type: none"> <li>➤ Logic micro-operations</li> <li>➤ Implementations and applications</li> </ul> </li> <li>• Shift micro-operations <ul style="list-style-type: none"> <li>➤ Logical shift, circular shift, arithmetic shift</li> <li>➤ Combinational circuit shifter</li> </ul> </li> <li>• Arithmetic logic shift unit</li> </ul>	
3.	Fundamental of Computer Organization and Design	7

	<ul style="list-style-type: none"> <li>• Computer Register <ul style="list-style-type: none"> <li>➤ Registers for the basic computer and common bus system</li> </ul> </li> <li>• Computer instructions <ul style="list-style-type: none"> <li>➤ Instruction format, basic instructions, instruction set completeness, types of instruction (memory reference, register reference, I/O)</li> </ul> </li> <li>• Instruction cycle <ul style="list-style-type: none"> <li>➤ Phases of instruction cycle</li> <li>➤ Fetch and decodes</li> <li>➤ Flowchart for instruction cycle</li> </ul> </li> <li>• Input and Output and Interrupt <ul style="list-style-type: none"> <li>➤ I/O configuration, Input-output instruction</li> <li>➤ Types of interrupt, Program interrupt, Interrupt cycle</li> </ul> </li> <li>• Basic computer design and accumulator logic <ul style="list-style-type: none"> <li>➤ Basic hardware components</li> <li>➤ Flowchart for computer operation</li> <li>➤ Control logic gates</li> <li>➤ Control of register and memory</li> <li>➤ Control of common bus</li> <li>➤ Control of flip-flop</li> <li>➤ Design of accumulator logic (control of AC register, Adder and Logic circuit)</li> </ul> </li> </ul>	<p>1</p> <p>1.5</p> <p>1</p> <p>1.5</p> <p>2</p>
4.	Control Unit	5
	<ul style="list-style-type: none"> <li>• Control Memory <ul style="list-style-type: none"> <li>➤ Control Word, Control memory, Stored program organization</li> </ul> </li> <li>• Hardwired control <ul style="list-style-type: none"> <li>➤ Introduction, Timing and control, Control unit of basic computer, Timing signal</li> </ul> </li> <li>• Micro-programmed control <ul style="list-style-type: none"> <li>➤ Micro-program control organization</li> <li>➤ Address sequencing <ul style="list-style-type: none"> <li>▪ Introduction, Conditional branching, Mapping of instructions, Subroutines</li> </ul> </li> <li>➤ Micro-programs <ul style="list-style-type: none"> <li>▪ Micro-instruction and micro-operation format, Symbolic micro-instructions, Symbolic micro-program, Binary micro-program</li> </ul> </li> </ul> </li> <li>• Design of control unit <ul style="list-style-type: none"> <li>➤ F-field decoding, Micro-program sequencer</li> </ul> </li> </ul>	
5.	Central Processing Unit	
	<ul style="list-style-type: none"> <li>• Register Organization <ul style="list-style-type: none"> <li>➤ Bus system of CPU, Control word, ALU and Micro-operation for CPU</li> </ul> </li> <li>• Register Stack and Memory Stack <ul style="list-style-type: none"> <li>➤ LIFO and Stack pointer, Register stack, Memory stack</li> </ul> </li> <li>• One address and two address instruction <ul style="list-style-type: none"> <li>➤ Instruction format, One address instruction, Two address instruction, Three address instruction, and Zero address instruction</li> </ul> </li> <li>• Addressing modes <ul style="list-style-type: none"> <li>➤ Introduction, Implied mode, Immediate mode, Register mode, Register</li> </ul> </li> </ul>	

	<p>indirect mode, Auto-increment/Auto-decrement mode, Relative address mode, Indexed addressing mode, Base register addressing mode</p> <ul style="list-style-type: none"> <li>• Data transfer and Manipulation <ul style="list-style-type: none"> <li>➤ Basic operations</li> <li>➤ Data transfer instructions</li> <li>➤ Data manipulation instructions <ul style="list-style-type: none"> <li>▪ Types, Arithmetic instructions, Logical and bit manipulation instruction, Shift instruction</li> </ul> </li> </ul> </li> <li>• Introduction to RISC and CISC <ul style="list-style-type: none"> <li>➤ Introduction to RISC and CISC, Characteristics of RIAC and CISC, Overlapped Register Window</li> </ul> </li> </ul>	
6.	Fixed Point Computer Architecture	5
	<ul style="list-style-type: none"> <li>• Addition and Subtraction <ul style="list-style-type: none"> <li>➤ Introduction, Addition and Subtraction with signed magnitude, Hardware Implementation, Hardware Algorithm</li> <li>➤ Addition and Subtraction with signed 2's complement</li> </ul> </li> <li>• Multiplication <ul style="list-style-type: none"> <li>➤ Introduction, Hardware Implementation and Algorithm, Booth algorithm, Array multiplier</li> </ul> </li> <li>• Division Algorithm <ul style="list-style-type: none"> <li>➤ Introduction, Hardware implementation, Overflow, Hardware algorithm, Restoring method, Comparison and non-restoring method</li> </ul> </li> </ul>	1.5 2 1.5
7.	Input and Output Organization	6
	<ul style="list-style-type: none"> <li>• Introduction to Peripheral Devices <ul style="list-style-type: none"> <li>➤ I/O subsystem and peripherals</li> </ul> </li> <li>• I/O interface <ul style="list-style-type: none"> <li>➤ Interface I/O bus and interface module, Types of I/O commands</li> <li>➤ I/O and Memory bus, Isolated I/O, Memory mapped I/O, I/O interface unit</li> </ul> </li> <li>• Direct Memory Access (DMA) <ul style="list-style-type: none"> <li>➤ Types of I/O, DMA, DMA transfer</li> </ul> </li> <li>• I/O Processor <ul style="list-style-type: none"> <li>➤ I/O processing, CPU-IOP communication</li> </ul> </li> <li>• Data Communication Processor <ul style="list-style-type: none"> <li>➤ Serial and parallel communication, Data communication processor, Modes of data transfer, Protocol</li> </ul> </li> </ul>	0.5 1.5 1.5 1 1.5
8.	Memory Organization	6

<ul style="list-style-type: none"> <li>• Hierarchy of Memory System <ul style="list-style-type: none"> <li>➤ Types of memory, Sequential, Random, Memory hierarchy</li> </ul> </li> </ul>	1
<ul style="list-style-type: none"> <li>• Primary and Secondary Memory <ul style="list-style-type: none"> <li>➤ Primary memory – RAM, ROM, Bootstrap Loader, RAM and ROM Chips, Memory Address Map, Memory-CPU connection</li> <li>➤ Auxiliary Memory – Types, Magnetic (Tape, Disk), Optical, Semiconductor</li> </ul> </li> </ul>	1.5
<ul style="list-style-type: none"> <li>• Virtual Memory <ul style="list-style-type: none"> <li>➤ Introduction, Address space, Memory space, Address mapping using pages, Associative page table, Page replacement</li> </ul> </li> </ul>	2.5
<ul style="list-style-type: none"> <li>• Memory management hardware <ul style="list-style-type: none"> <li>➤ Introduction, Segmented page mapping, Memory protection</li> </ul> </li> </ul>	1

Text Books: M. Morris Mano, Computer System Achitecture

References:

M. Morris Mano “Digital Design”, Pearson Education, Third Edition

M. Morris Mano “Logic and Computer Design Fundamentals”, Pearson Education, 2<sup>nd</sup> Edition Updated.

Members:

Dr. Subarna Shakya-----Expert/Coordinator

Hari Khadka-----Patan Campus

Bhoj Raj Ghimire-----Amrit Science Campus

A.N. Mishra-----St. Xavier College

Pratima Karki-----Kathford College